Patent Case Text

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FIELD OF THE ART

The present invention relates to the field of signal processing and frequency synthesizer and communication transceiver architectures, more particularly, the present invention relates to a synthesizer, and in particular a synthesizer with PLL and a clock generator based on mixed-signal waveform generation for multi-channels, multi-mode, multiple wireless and wire communications standards in a class of very compact and cost-effective architectures.

BACKGROUND DESCRIPTION OF THE RELATED ART

A communication system transfers information between a source and a destination. Generally, a communication system includes at least one transmitter and one receiver which transmit and receive information signals over some media, respectively. This media may be cable wiring or no wiring, like atmosphere. When communications occur

over no wiring, they are commonly referred to as "wireless" communications. Examples of wireless communications systems include wireless modems, digital cellular, digital cordless telephones, wireless local and wide area networks, digital satellite communications and personal communications networks. This invention is related to frequency planning, frequency synthesizer and transceiver architectures for communication standards like IEEE802.11 a/b/g WLAN ,Bluetooth, WCDMA, GSM quad-band, and CDMA dual-band etc....

Communication transmitters are usually in direct conversion. The receivers have a number of different architectures, including multi-stage and direct conversion. These approaches have a number of different problems associated with them. For example, in multi-stage approaches, the low intermediate frequency (IF) required for use with certain filters results in an image channel that is fairly dose to the desired RF signal. To compensate for this close image channel, the receiver requires a sharp image-rejection filter in the front-end in order to provide enough image suppression prior to mixing. Direct conversion architectures can be designed so that the image signal and the desired channel are essentially the same so that there is no need for an image rejection filter. However, imperfect isolation between the local oscillator (LO) and the antenna results in the LO signal being detected by the antenna, thereby producing a DC component at the output of the receivers. Also, most of the signal amplification is usually performed at the base-band and consequently the signal level at the input of channel-selection filters may be low enough to be completely masked by the 1/f noise. The frequency plan and synthesizer design provide the possibility to adapt all the possible architecture mentioned

above, either in transmitter and receiver sides for different circuit device process technology.

In many modern wireless communication standards, the bandwidth is partitioned into many channels with certain carrier frequencies. Synthesizers are used in communication devices to obtain an output signal that is synchronized with some other signal, such as reference signal to generate signals with those frequencies. Certain synthesizers use what is known as phase locked loop (PLL) with programmable dividers and a voltage controlled oscillator (VCO) to cause the output signal frequency to vary in dependence upon the input control voltage. In this traditional approach, the frequency synthesizer, VCO tuning range, frequency divider locking range needs to be extended as bandwidth and channel number increase. And the channel switching capability need more complicated design to meet the lock control, stability, phase noise, channel switching lock-in time and power consumptions etc...requirements.

BRIEF SUMMARY OF THE INVENTION

The invention provides the frequency plan, frequency synthesizer and transceiver architectures to be easier for fine tuning to meet the system requirements. As more communication standards are integrated into a single mobile device, the invention provides a single transceiver device to have multi-mode or multiple standard frequency channels access capability with one single frequency synthesizer. Furthermore, the invention provides a compact and cost-effective frequency synthesizer architecture for multi-port communication systems like WLAN IEEE802.11a/b/g access points, 3G wireless base-station or one with any and any combination of standards in Table.1 or claim2.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide frequency plan and architectures for the frequency synthesizer and transceiver to meet multiple wireless communication standards at one frequency planning design, especially with instant and simultaneously channel switching capability, which is difficult for the traditional frequency synthesizer with programmable divider mentioned in above prior art. The invention also provides a cost-effective for multi-port WLAN or 3G wireless base stations. The invention will also provide the new and cost-effective wireless device to enable next generation wireless network with fast and simultaneously channel switching capability to improve the communication efficiency and make the other wireless RF circuits blocks easier for implementations.

It is another object of the present invention to provide a method of and apparatus for generating different frequency signals for synthesizing the desired frequency signal with robust and simple circuit implementations.

It is another object of the present invention to provide a method to systematically obtain a pure spectrum carrier frequency signals based on main constant frequency source to meet multiple communication standards requirement and easily fine tune the phase noise performance to meet the requirement of various wireless communication system.

The present invention attains at least the above objects, and others, either singly or in combination, by providing a synthesizer having an instant/simultaneously channel switching lock condition without the traditional programmable divider. This allows for a method of operating the synthesizer, methods of establishing or reestablishing a lock condition using a frequency source like a fine tuned single frequency VCO without complicated design to extend the frequency tuning range of the VCO. It also enables the utilization of a high radio frequency source such as micromachining oscillators with less phase noise to meet the advanced wireless communication system requirement.

Advantages of each of the above-recited aspects of the present invention will become apparent in the discussion provided hereinafter.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objectives, features, and advantages of the present invention are further described in the detailed description which follows, with reference to the drawings by way of non-limiting exemplary embodiments of the present invention, wherein like reference numerals represent similar parts of the present invention throughout several views and wherein:

FIG. 1 is a block diagram of one embodiment of frequency synthesizer of the front-end circuitry for use in a communications device.

FIG. 2This exemplary design is dedicated to direct conversion transceiver.

FIG. 3This exemplary design is dedicated to a direct conversion transmitter and a multi-stage down-conversion receiver.

FIG. 4 illustrates a conventional PLL circuit that uses a VCO to generate the two main classes of constant frequencies f1 and f2.

FIGS.5 quadrature superharmonic frequency dividers

FIG.6 Architecture of the mixed-signal waveform clock generator

FIGS. 7 illustrate the frequency mixer architectures according to the present invention;

FIG. 8 This exemplary design is a direct conversion transceiver dedicated to the GRFS to support multi-mode IEEE802.11a/b/g WLAN transceiver and Bluetooth.

FIG. 9 This exemplary design is a direct conversion transmitter and High-IF multi-stage receiver dedicated to the GRFS to support multi-mode IEEE802.11a/b/g WLAN transceiver and Bluetooth.

FIG. 10 This exemplary design is a direct conversion transmitter and Low-IF multi-stage receiver dedicated to the GRFS to support multi-mode IEEE802.11a/b/g WLAN transceiver and Bluetooth.

FIG. 11 This exemplary design is dedicated to a multi-port transceiver sharing the same f1 and f2 frequency generators.

DETAILED DESCRIPTION OF THE INVENTION

The present invention shown in FIG.1 provides a synthesizer for use in multi-mode, multi-standard and multi-port communication devices, which, unlike conventional synthesizers, uses a PLL with a VCO to cause an output signal frequency to vary in dependence upon an input control voltage and programmable frequency dividers. The frequency synthesizer is composed of one single constant high radio frequency generator based on PLL and dividers as shown in FIG.5 to generate two classes of frequencies f1 and f2 in FIG 4 and a mixed-signal f3 frequency generator in FIG. 6 to provide instant and simultaneously channel switching lock capability. Those aspects of the present invention that differ from a conventional synthesizer will accordingly be described hereinafter, with the conventional PLL single frequency generator portions not being described in detail. Furthermore, the high frequency generator for f1 and f2 is not necessarily generated by traditional VCO circuits, it can use oscillators with frequency dividers made by Micromachining device and other stable frequency reference to meet the communication system requirement such as phase noise and power consumptions. And the mixed-signal f3 waveform synthesizer can also be a direct digital frequency synthesizer (DDFS) circuits which need more complicated design and power consumption.

As mentioned above, it is desirable to generate fast channel switching lock within one communication standard or among different communication standard and meet the phase noise requirement. This invention can simplify the design complexity and meet the spec. requirement easily by the well frequency planning invention. In Table .1 we show the

frequency planning for multiple wireless communication standards based on this invention. A 20MHz reference crystal oscillator is used as a reference to generate the desired 5280MHz from the first PLL frequency generator with a constant divided-by-264 divider consisted of three divide-by-two circuits, one divided-by-three, and one divided-by-eleven circuit as shown in FIG.4. And the 2640MHz signal is generated by a quadrature injection locking divided-by-two circuit with the 5280MHz signal as input. With the constant frequency divider operations, the 5280MHz/M, M=1,2,3,4,6,8,16,48, frequencies are generated to be synthesized with f3 for multi-mode and multi-standard wireless communication systems. As shown in Table 1. The f3 frequency ranges of the mixed signal waveform generator are optimized for all the wireless communications system on the list. It is a dedicated design of the non-linear mathematic COS and SIN waveform generator for f3 frequency generation without any big memory device which consumes a lot of area and power inside the tradition direct digital frequency generator. And the DAC cell is fine tuned to the non-linear value according to the sinusoidal waveform. The positive and negative frequency of f3 is depended on the positive and negative summation operation of the channel selection control bits in FIG.6. The frequency summation operations are based on dual inputs balanced mixer or triple inputs balanced mixer as shown in FIG.7 shown in CMOS topologies. With the above preferred circuit embodiment implementation, they can be applied in direct conversion, low-IF and high-IF transceivers as sown in FIG.8 FIG.9 and FIG10.

The invention can be used as a single carrier fc frequency synthesizer for not only a single standard multi-mode device but also multi-mode and multi-standard device as shown in FIG. 1 according to the frequency plan in Table.1 such as a combo

IEEE802.11a/b/g, Bluetooth, WCDMA, CDMA dual-band, GSM quad-band, and GPS transceivers. The channel switching time is almost zero in this frequency synthesizer architecture. It can also be used as multiple ports frequency synthesizers in not only a single standard multi-mode communication system but also multi-mode and multi-standard system by adding more f3 frequency generators without adding more f1 and f2 frequency generators as shown in FIG. 11. The f1=5280MHz frequency generator can also be used with constant frequency generators for generating the 11MHz,22MHz,44Mz,88MHz clocks for the IEEE802.11b/g and cable modem applications. That is, this frequency planning and frequency synthesizer architecture is also fit for a broadband gateway or routers with wireless links. By this invention, the frequency synthesizer design can be very compact and cost-effective in various communications networking systems.

Although the present invention has been described in detail with reference to the preferred embodiments thereof, those skilled in the art will appreciate that various substitutions and modifications can be made to the examples described herein while remaining within the spirit and scope of the invention as defined in the appended claims.

Unit:MHz	f1 : Direct Conversion Multi-stage	f2	f3
IEEE802.11a Lower 5G Band 5180:20:5320	5280 4620=5280-660	0 660	-100:20:40
IEEE802.11a Upper 5G Band 5745:20:5805	5940=5280+660 6600=5940+660	0 -660	-195:20:-135
IEEE802.11b/g 2412:5:2472	2420=5280/3+660 3080=2420+660	0 -660	-8:5:52
Bluetooth 2402:2480	2420 3080	0 -660	-18:1:60
WCDMA BS:1920:5:1980 MS:2110:5:2170	1980=5280/4+660 1320=5280/4	0 660	-60:5:0
	2090=5280/3+660/2 1430=5280/3-660/2	0 660	20:5:80
GSM Quadband 869:894	880=5280/6 1540=880+660	0 -660	-11 : 0.2 : 14
925:960	880 1540	0 -660	45:80
1805:1880	1870=5280/3+660/6 1210=1870-660	0 660	-65:10
1930:1990	1980=5280/4+660 1320	0 660	-50:10
824:849	880 1540	0 -660	-56 : -31
880:915	880 1540	0 -660	0:35
1710:1785	1760=5280/3 1100=1760-660	0 660	-50:25
1850:1910	1870=5280/3+660/6 1210=1885-660	0 660	-20:40
CDMA Dualband celluar 824:925	880 1540	0 -660	-56:45
PCS:1750:1980	1870 1210	0 660	-120:110

Table 1. Frequency Plan of frequency synthesizer and transceiver for wireless communication networking systems.